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Research Article
Design of AC-Coupled Circuit for High Speed Interconnect Using Pass Transistor

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Keywords

Pass Transistor, three-dimensional integrated circuit (3D IC), AC-Coupled, high-speed interconnected, differential signal transmission.

Abstract

The scaling of semiconductor technology together with 3D IC stacking integration make it possible for many portable electronics to process large amount of multimedia data.AC coupling enables chip placed face-to-face for signal transmission using close field capacitive coupling. A high performance system design using AC coupled interconnect (ACCI) technology achieves shorter and faster interconnection . This paper describes the Pass Transistor based chip-to-chip circuit design suitable for high-speed 3DIC interconnected applications. The AC-Coupled face-to-face (F2F) chip was simulated using HSPICE under a 1.8 V supply voltage

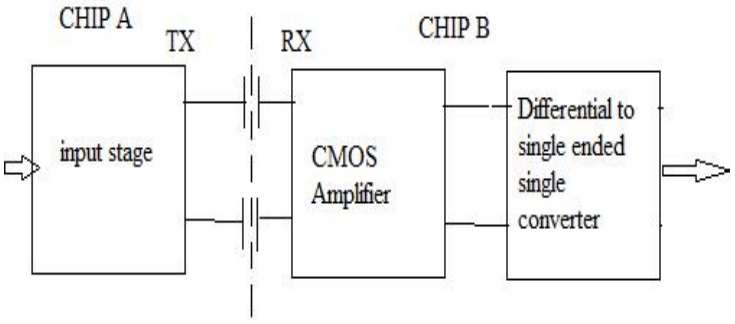
Introduction

With CMOS technology continuing to scaling down, the conventional copper (Cu) based electrical interconnect cannot longer satisfy the IC and packaging design specifications for lower delay, lower power, higher bandwidth, and lower noise requirements. In addition, the complexity of ICs continually dominates the device speed performance. As the scale of CMOS manufacture technology increase significantly in each new technology, interconnection delays have become dramatically significant for 0.18 m technology node. In order to keep up with Moor's law scaling and to meet application demands, the three-dimensional integrated circuit (3DIC) integration has been an attractive solution to complex integration due to its higher number of I/O pin counts, wide communication parallelism and heterogeneous integration in the packaging. An alternative to metal wiring interconnections, proximity communication (PxC) or contactless communication can be realized with capacitive coupling interconnection (CCI) or inductive coupling interconnection (ICI) methods. An ICI [8] is the current driven and allows for long-distance communications between two chips. The communication capability of inductive coupling is increased the driven current or the layout area of inductor. In addition, the ICI basically requires stacked vertical structure and separate interfaces which also increase the area overhead [8]. In contrast, CCI is the voltage driven and its structures are applying the near-distance communications in face-to-face (F2F) stacking.

The above diagram is the block diagram of this paper. It contains the input stage, CMOS Amplifier and differential single ended single converter. And it has 2 Chips, Chip a and Chip b. Input stage is the transmitter circuit and CMOS amplifier, differential single ended single converter is the receiver circuit.

Existing system

The schematic of the proposed CCI transceiver, which include a transmitter (Tx) and receiver(Rx) is shown in figure. A three stage CCI is designed using 1P6M 0.18 m CMOS technology provided by TSMC with 1.8 volts power supply. The receiver (Rx) circuit consists of a pre-amplifier, input DC voltage bias (VB), a loopback transmission-gate, a digital signal amplifier, and a digital comparator. The input stage of the receive circuit includes CMOS pre-amplifier inverters (Mp4/Mn4, Mp5/Mn5) and transistors MP6~9 and MN6~9, senses differential signal pluses and converts them into single- end signal pulses. The CMOS pre-amplifier inverters have a large (negative) gain when its input is biased to 0.9 V (VDD/2). These four transistors (MpR12~13 and MnR12~13) perform as negative feedback resistors whose resistance value are adjusted by an input DC bias VB. In the stage, the transmission-gate function as negative feedback (MpR12~13 and MnR12~13) path can clamp the input bias at the point of half supply voltage such



. Schematic for A capacitive coupling interconnection

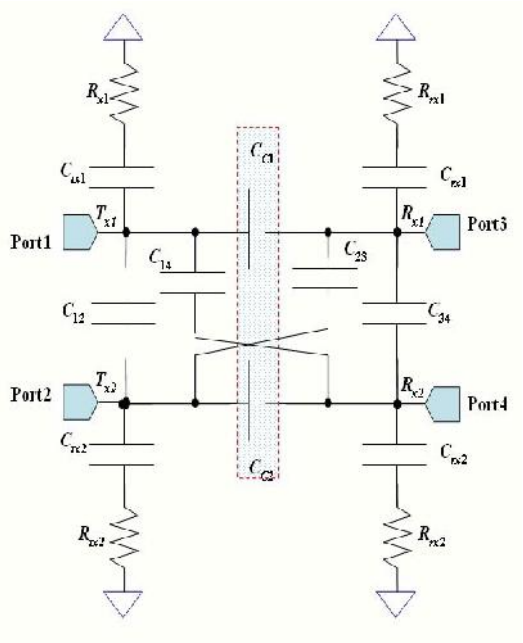


Fig. 2. Idealized model for analyzing the physics of capacitive coupling between two pads

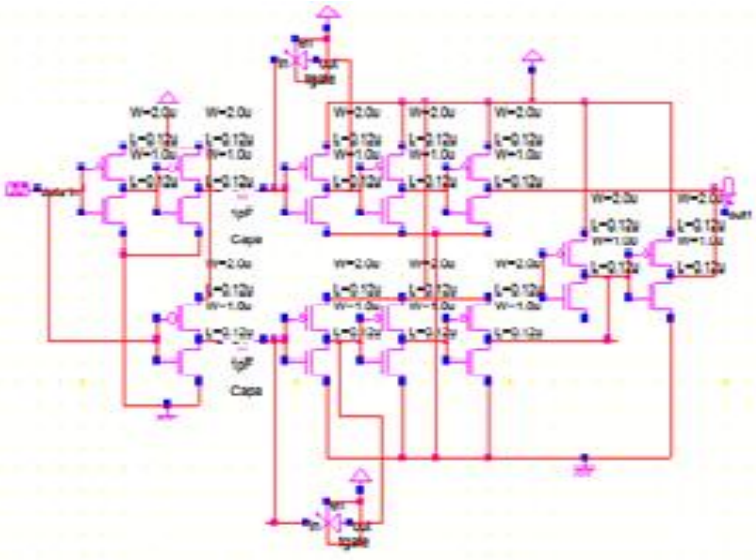


fig3.Schematic for existing ac coupled interconect

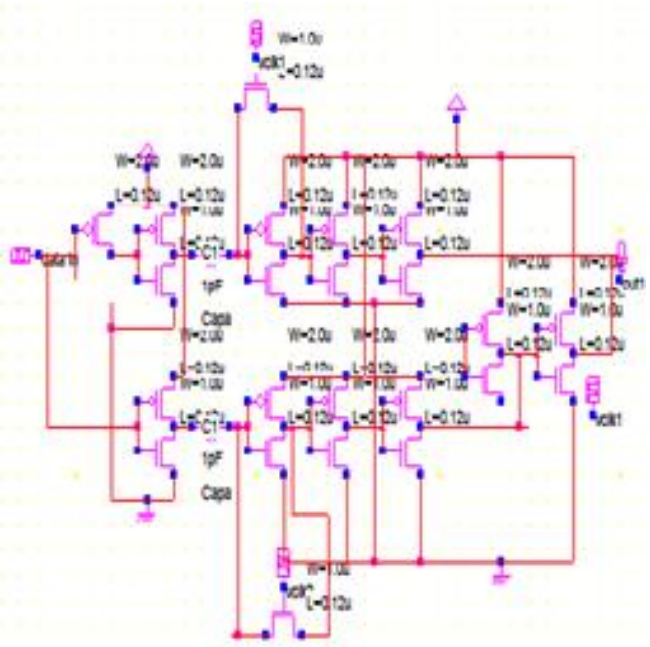
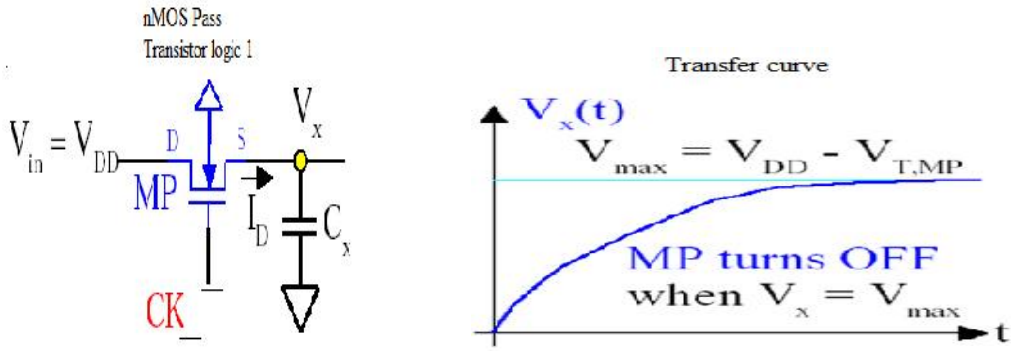
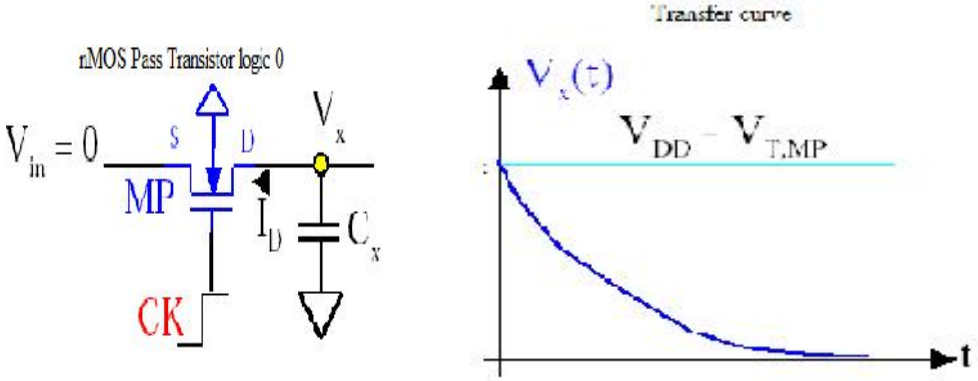


fig4.Schematic for proposed ac coupled interconnect

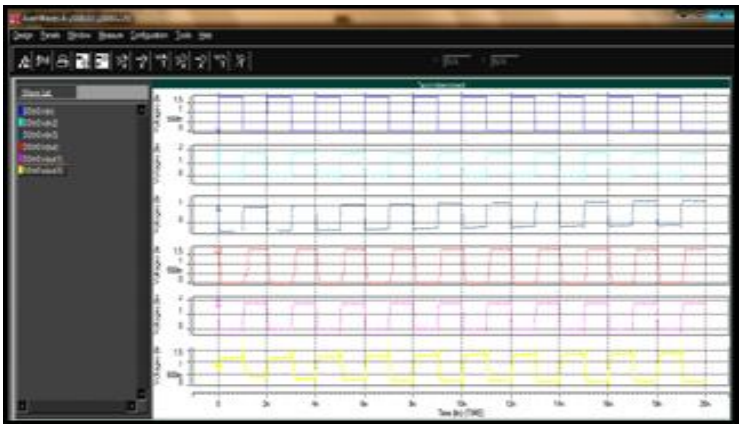


$$V_{max} = V_x(t)\big|_{t=\infty} = V_{DD} - V_{T,MP}$$

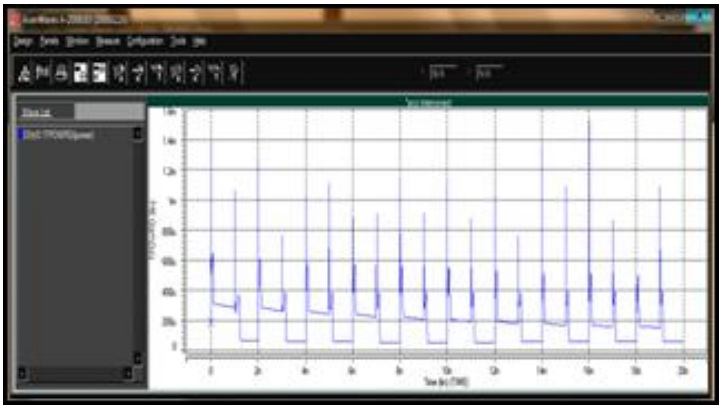


Existing System

Voltage vs Time

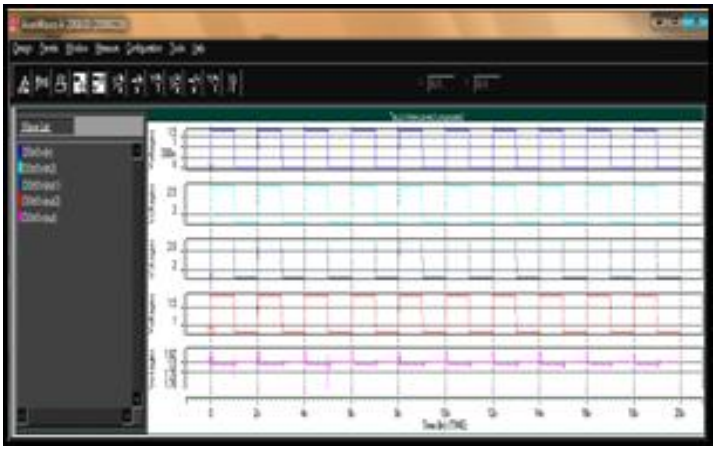


Power

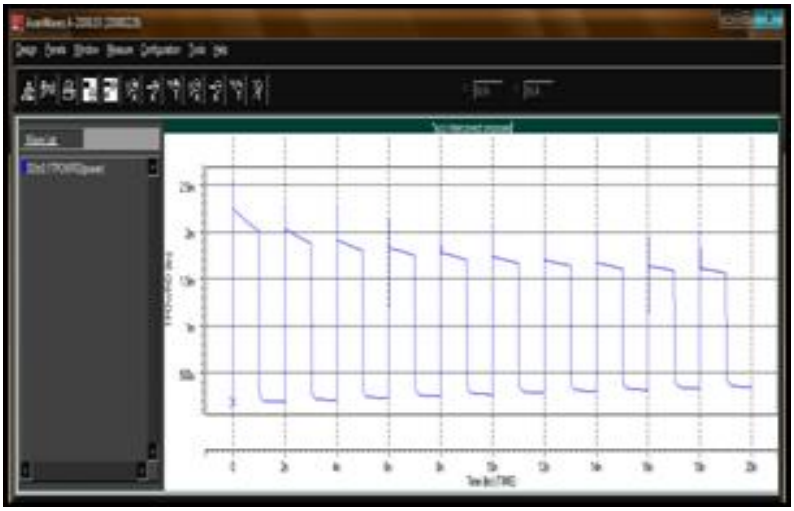


Proposed System

Voltage vs Time



Power



Observation table

FACTOR	EXISTING SYSTEM	PROPOSED SYSTEM
TOTAL CPU TIME	2.66 SEC	1.90 SEC
TOTAL ELAPSED TIME	3SEC	2 SEC
TOTAL MEMORY USED	178 KB	177 KB

that inverter Mp4/Mn4 and Mp5/Mn5 can behavior as amplify and obtain the largest small-signal gain. The next stage, the receiver circuit of the cross CMOS inverter (Mp10/Mn10 and Mp11/Mn11) can be used to reduce inverter (Mp10/Mn10 and Mp11/Mn11) can be used to reduce the noise. The differential driver with tapped buffer inserted can drive the output pad around 1 pf and converts input signals into full swing digital signals for digital scope measurement. The CMOS inverter and feedback transmission-gate at the receiver-end can be used to control the high-gain signal effect of amplification.

Proposed system

The Schematic of the proposed CCI transceiver, the feedback Pass Transistor at the receiver end can be used to increase the performance speed and reduce the area of the circuit. A three stage CCI is designed using 1P6M 0.18 m CMOS technology provided by TSMC with 1.8 volts power supply. The receiver (Rx) circuit consists of a pre-amplifier, input Vclk for pass tansistor, a digital signal amplifier, and a digital comparator. The input stage of the receive circuit includes CMOS pre-amplifier inverters (Mp4/Mn4, Mp5/Mn5) and transistors MP6~9 and MN6~9, senses differential signal pluses and converts them into single- end signal pulses. The 'pass transistor' perform as negative feedback resistors whose resistance value are adjusted by an input Vclk. In the stage, the pass transistor function as negative feedback (Mn12,Mn13) path can clamp the input bias at the point of half supply voltage such that inverter Mp4/Mn4 and Mp5/Mn5 can behavior as amplify and obtain the largest small-signal gain.

The next stage, the receiver circuit of the cross CMOS inverter (Mp10/Mn10 and Mp11/Mn11) can be used to reduce inverter (Mp10/Mn10 and Mp11/Mn11) can be used to reduce the noise. The differential driver with tapped buffer inserted can drive the output pad around 1 pf and converts input signals into full swing digital signals.

Pass transistor

Pass transistors are very efficient in use of transistor, potentially very efficient layout result. Use of CMOS transmission gate circumvents the Vtn voltage drop of nMOS pass transistor. Dynamic power may be decreased.

Simulation result

The CMOS inverter and feedback Pass transistor at the receiver-end can be used to control the high-gain signal effect, reduce the area and increase the system speed. The simulation results are performed at VDD=1.8V at different temperatures -40.

The testing signal input to the Tx node is transmitted to the Rx node using CCI coupling interconnection. The simulation results of the testing signals transmitted at different nodes are depicted in Figure. The input signals intend adding noise signal are subtracted away by the proposed circuit with a differential receiver.

Conclusion

In this work a difference CCI is designed using HSPICE with 1.8 volts power supply. The total cpu time required to execute this circuit is too minimum and the total elapsed time also much less. The simulation results indicated the proposed circuit not only has the self-test characteristics but also is suitable for high-speed interconnected applications with differential signal transmission up to 2.5 Gbps.

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