Research Article

Implementation of high performance image scaling processor using VLSI

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Abstract

A system with low cost& low power consumption is considered as efficient. So our project deals a with nearest neighbour algorithm in order to reduce the size of the memory. Dynamic estimation unit is used in order to reduce the cost in Dynamic estimation unit SPST is used. The pre- filters are used to reduce the aliasing artefacts caused by bilinear interpolation. A T-model inversed T-model and convolution kernels are proposed to make the design as less complex. It is implemented in the Xilinx 9.2i & model sim simulator.

I. Introduction

Isan important process in medical field and aero research centers in this fields digital cameras. Digital image processing has a wide range of application related to our day to day life such as remote sensing, space exploration and medical image applications etc..The image scaling is an important concept in the digital image processing and adopted in electronic devices such as recorders , and digital photon frames,. An image scaling is applied when variable size images are delivered to users from different multimedia sources. When the resolusion of the received image is low, the user needs to magnify the image and display it via the high resolution display devices .However ,resizing the image would produce severe jagging and blurring in the image.

It has become a significant rend to design a low-cost, high quality ,and high performance image scalar by VLSI technique for multimedia electric products. The image scaling is done by means of applying image interpolation methods. Image interpolation is that a method to increase or decrease the number of pixcels in a digital image. Image interpolation is of two types namely adaptive interpolation and non –adaptive interpolation . Various non adaptive algorithms are proposed for the image scaling ,the nearest neighbour algorithm is the simplest method with low complexity and easy implementation .

The image produced using this algorithm consists of full of blocking and aliasing artefacts. The bilinear interpolation uses linear interpolation to calculate the unknown pixcel value. Bilinear interpolation algorithm is used in most of image scaling processor due its low complexity, ease of implementation and image quality.

II. Proposed scaling algorithm

A filter is used as the pixels of the original input image to remove the noise and also enhances the edges. They help in reducing the blurring and aliasing artifacts produced by the bilinear interpolation algorithm. And also removes the unwanted discontinuous edges and boundaries. There are two filters combined to produce the combined filter.
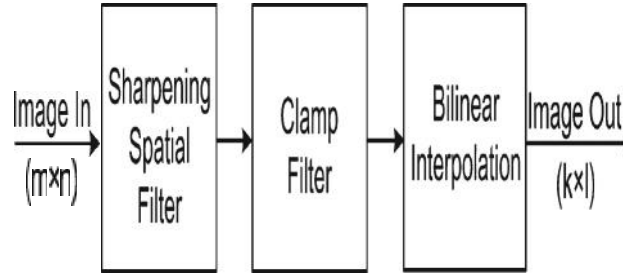

Block diagram of the proposed scaling algorithm for image zooming.

A)   Less complexity sharping filter

The filter is a kernals that is used to increase the intensity of the centers and their neighboringpixcels. The spatial filter is a high pass filter and clamp filter is a low pass filter. Clamp filters are the 2-D Gaussion spatial domain filters. It is composed of arrays. It having a single + value at the center and fully surrounded by 1.when the convolution is increase the image quality is increased. Convolution filter are demands large size and more memory, hardware cost.
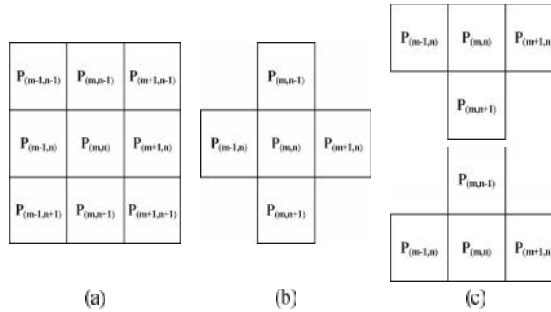
Cross-model 2.Weights convolution of the convolution kernel. (kernels.c) T-model (a) and 3 × convolution T-model kernel. Convolution kernels.

For eg:6*6 convolution filter needs a five line buffer memory and 36 arithmetic unit which is much higher than the one line buffer memory. In the proposed work each of the filters can realized by a 2D 3*3 convolution kernal.It needs 4-memory for 2(3*3) convolution filters. It reduce the complexity ofthe kernals, cross model form is used to replace 3*3 convolutionkernal. It decreases the memory and complexity of the kernals. Cross model form is used to replace 3*3 convolution kernal.It decreases the memory and complexity T-model and inversed T-model is composed the lower 4 parameters and upper 4 parameter respectively and to enhance the image quality in the proposed scaling algorithm T – model and inversed T model provides a low complexity and memory requirement for the sharping filters to integrate the vlsi chip of the proposed ,low cost image scaling processor.

B) Combined filter

In the proposed algorithm, input image is first filtered using a clamp and spatial filters. It still requires two line buffers for storing the input data.The intermediate values for each T model or inversed T model filter. The able to decrease the computing resource and memory requirement. The combined filter formed the T model or inversed T model is used in the sharping spatial and clamp filter.

The parameters S and C are the spatial and clamp filters. The reduce the one line buffer memory two only parameter in the third line. The P(m,n-2) is the

removed .This filter combination technique ,memory requirement can be decreased from two to one line buffer.

$$P'_{(m,n)} = \left[P^*_{(m,n)} \begin{bmatrix} -1 & S & -1 \\ & -1 & \end{bmatrix} / (S-3) \right]^* \begin{bmatrix} 1 & C & 1 \\ & 1 & \end{bmatrix} / (C+3)$$

$$= P^*_{(m,n)} \begin{bmatrix} -1 & S-C & SC-2 & S-C & -1 \\ & -2 & S-C & -2 & \\ & & -1 & & \end{bmatrix}$$
$$/ \left[(S-3) \times (C+3) \right]$$

$$\approx P^*_{(m,n)} \begin{bmatrix} -1 & S-C & SC-2 & S-C & -1 \\ & -2 & S-C & -2 & \end{bmatrix}$$
$$/ \left[(S-3) \times (C+3) \right]$$

III. Block diagram

This section gives a brief description about prefilters and bilinear interpolation. Fig.1 shows the block

diagram of image scaling algorithm. The sharpening spatial filter andclamp filter serves as prefilters to the bilinearinterpolation, to reduce the blurring and aliasing effects.
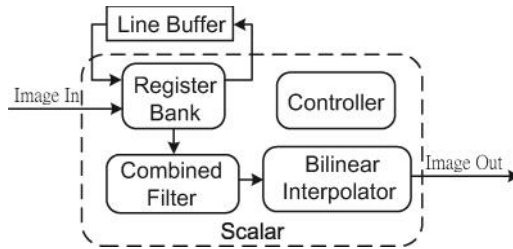
*Block diagram of image scaling processor*

A)   Line buffer

SEPD adopts a 3*3 mask,so three scaning lines are needed.If p(i,j) are processed,threepixcels from row(i-1),row I and row (i+1),are needed to perform the desioningprocess.With three scannng lines with two line buffers.There are designed to store the piixcels at odd and even rows,respectively.To reduce cost and power consumption ,the line buffer is implemenated with a dual –port SRAM instead of a series of shifter registers. If the size of an image is Iw *Ih, the size required for one line buffer is Iw -3 bytes in which 3 represents the number of pixcels stored in the register

bank.The each   value stored in other   registers belonging to row n+1will be shifted right in to the next register or line buffer memory.

B) Register bank

The register bank is defined with a one line buffer memory .It is provide the ten values for the immediate usage of the combined filter. The architecture of the register bank with the structure of ten shift registers. When the shifting control signal is produced form the controller.
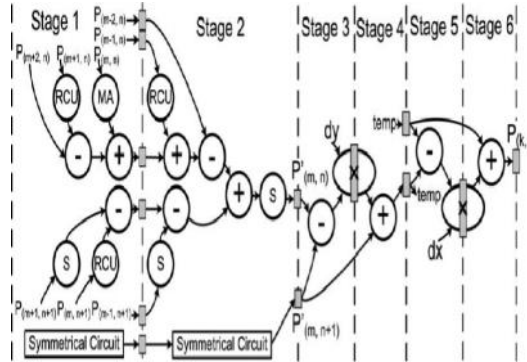

Architecture of the register bank.

48
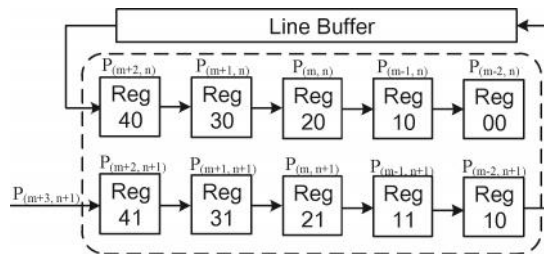
C) Combined filter

It minimized path delay to improve the performance by using the pipeline technology. The T model and

inversed T model filters has three Reconfiguration calculation unit, one multiplier, adder, three subtracts and three shifters are used in the circuit.

*Computational scheduling of the combined filter and Simpilified bilinear interpolator*

The stages 1 and 2 show the computational scheduling of a T-model combined and an inverse Tmodelfilter. The T-model or inversed T-model filter consists of one multiplier–adder, three reconfigurable calculation units, three adders (+), three subtracters (−), and three shifters. The values of the ten source pixels can be obtained from the register bank as mentioned earlier. The T-model and the inversed T-model are used to obtain the values of P'(m, n) and P'(m, n+ 1) simultaneously. The inversed T-model combined filter is represented by means of symmetrical circuit which is similar to symmetrical structure of the T-model combined filter, for producing thefiltered result of P'(m,n+1). The MA can be implemented by a multiplier followed by an adder.

A) Reconfigurable calculation unit

The RCU is designed to produce the calculation functions of (S-C) and (S-C-1) times of the source pixel value, which must be implemented with C and S parameters. According to the characteristics of the images, the C and S parameters values can be set by the users. Fig.7 shows the architecture of the RCU. It consists of four shifters, threemultiplexers (MUX), three SPST adders, and one sign circuit. The three adders use the SPS technique to reduce the power dissipation in the combinational VLSI design.

PPARAMETERS AND CCOMPUTING RRESOURCE FOR RCU

Parameters	Values	Computing Resource
C	5, 13, 29	Add and Shift
S	7, 11, 19	Add and Shift
S-C	2, -6, -22, 6, -2, -18, 14, 6, -10	Add, Shift, and Sign
S-C-1	1, -7, -23, 5, -3, -19, 13, 5, -11	Add, Shift, and Sign
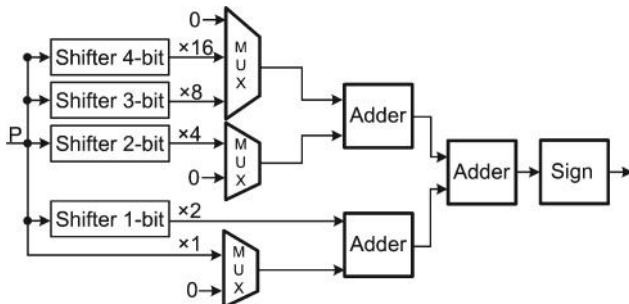
Architecture of RCU

49

B) Spurious power suppression technique (SPST)

The adders in the RCU design, uses spurious power suppression technique, are separated into two parts namely the most significant part (MSP) and the least significant part (LSP) between the eighth and the ninth bits. The adder is designed such that it latches the input data of the MSP whenever it doesn't affect the computation results. By eliminating the computation in MSP, it not only save power consumption inside the adder in the current stage but also reduce the glitching
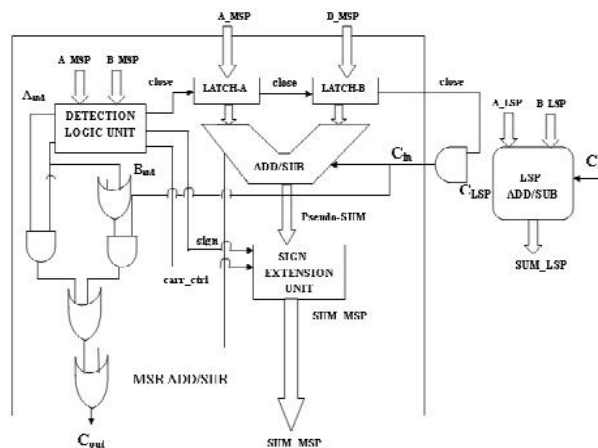
noises which occurs in the arithmetic units in the next stage. The detection logic unit and SE unit is used to determine the effective input ranges of the operands and used to compensate the sign signals respectively. The fig.8 shows the low power adder design adopting the SPST. The three output of the detection logic unit is that close, carr_ctrl and sign, the close value denotes whether the MSP circuit can be neglected or not during the computation.

When close value of zero is fed into the MSP circuit, the switching activities in the MSP circuit freezes, to avoid the dynamic power consumption. Thus when the value of close is zero, it indicates that the MSP circuits can be closed to save power dissipation. When the MSP is negligible, the input data of MSP becomes zero in order to avoid the glitching power consumption. The detection logic unit can decide whether the input data of MSB should be latched or not. The SE is implemented by multiplexers to compensate for the sign signals of MSP. The pseudo summation (PS) from the MSP adder is given as input to the SE. By this RCU design, the hardware cost of the combined filters can be efficiently reduced.

D) Bilinear interpolation

The bilinear interpolation method is selected because of it characteristics of high quality and low complexity. It is operation of 1st performs a linear interpolation in one direction and again interpolate other direction. Itcost eight multiply, four subtract and three additionoperations is used .Thus an algebraic manipulation has been used to reduce the computing resources of the bilinear interpolation.

Bilinear interpolator and controller

The four stage pipeline architecture is using a two stage stagePipeline Multipliers are used. To reduce the

delay path of the bilinear interpolator.The Input value is $p\_(m,n)$ and $p\_(m,n+1)$ are obtained from the combined filter and symmetrical circuit. The temperature result of the function $p\_(m,n) + dy* p\_(m,n+1) - p\_(m,n)$ can be replaced by the previous result of $p\_(m+1,n+1) + dy*p\_(m+1,n+1) - p\_(m+1i,n)$.The controller is implemented with finite stage machine circuit. It generatescontrol signalto control the time and pipeline stages. The registerbank, combined filter and bilinear interpolator. Thus reducing the power consumption.

IV. Power range used

In this work compare to previous ,usage of the power is reduced .The power range is 210mW.

V. VLSI Architecture

The above architecture shows the scaling algorithm proposed in this paper consists of two combined pre-filters: sharping spatial filter and clamp filter and one simplified bilinear interpolator .For VLSI implemention ,the bilinear interpolator can directly obtain two input pixcels from two combined pre filters without any line buffer memory.

VI. Simulation Result

As per the sSix stage pipeline architecure,the image is initally passed through the combined filter,where the alaising and blurring effects are removed. After that bilinear interpolation is performed on the filtered output to obtain a scaled image.The input image used for the image scaling process is jpg image. The image matrix is represented by 95 x 89 pixels, which totally contains 25365 bytes pixel values. T model and inversed T model matrix is produced as the output ofcombined filter.The filtered pixels p'(m, n) and p'(m, n+ 1) are given asinput to the bilinear interpolator. The fig.11 shows the bilinear interpolation output waveform with new scaled pixels. The scaled output image is displayed using the Matlab software. The output image of size 190 x178 is obtained. The total estimated power consumption of this image scaling algorithm is 303mW at a 115 MHz operating frequency and uses about 3.74-k gate counts with peak memory usage of about196MB.
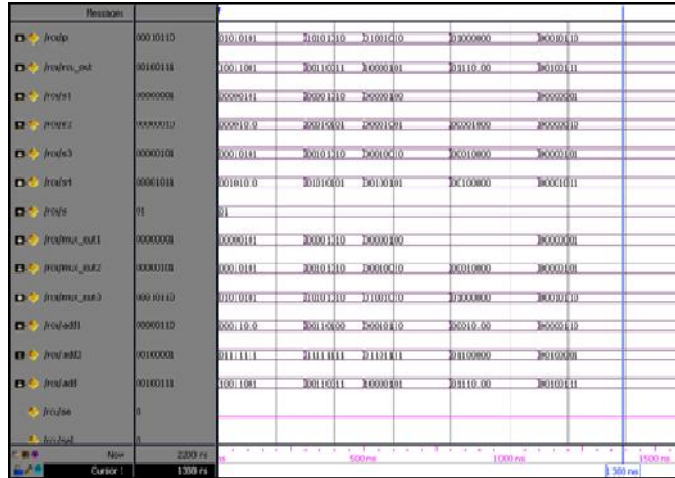
A)   Reconfigurable calculation unit waveform
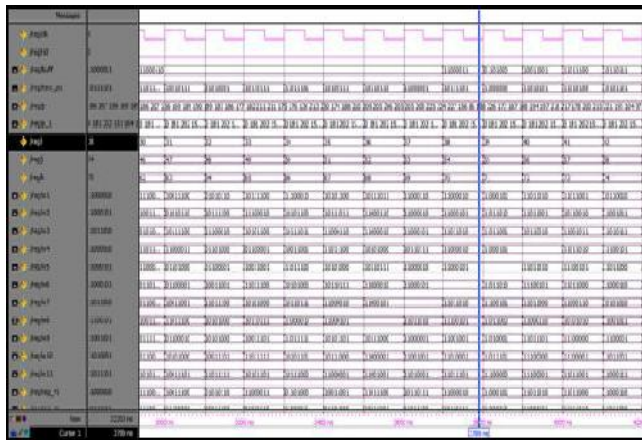
B) Bilinear interpolation output waveform with scaled pixel values
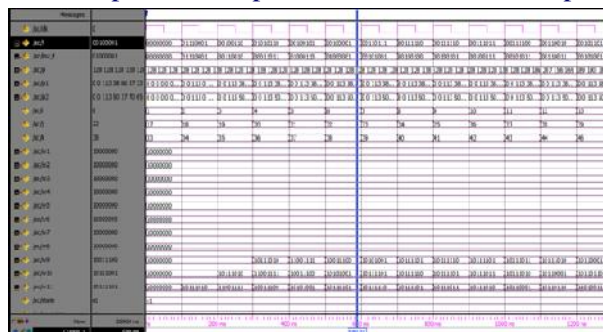
C) Combined filter output waveform with T model and inversed T model matrix

VII. Result

Xilinx ISE 9.2i is used for synthesis and implementation of a design . In order to evaluate performance of the proposed scheme first pixcel was calculated using MATLAB tool. From that binary equivalent of a pixcel is obtained, for FPGA implementation .FPGA is implementated in SPARTAN 3E.

VIII. Conclusion

In this work a low complexity,a low memory requirement ,high-performance and high quality VLSI architecture of the image scaling processor had been proposed. The spatial and clamp filter combining, sharing of hardware and reconfigurable techniques had been used to reduce the cost of hardware. Relative to the previous low-complexity VLSI scalar designs, this work achieves at least 34.5% reduction I gate counts and requires only one-line buffer. Usage of SPST adders reduces the power consumption to a great extent.

References

[1] K. Jensen and D. Anastassiou, "Subpixel edge localization and the interpolation of still images," *IEEE Trans. Image Process.*, vol. 4, no. 3 , pp. 285–295, Mar. 1995.

[2] H. Kim, Y. Cha, and S. Kim, "Curvature interpolation method for image zooming," *IEEE Trans. Image Process.*, vol. 20, no. 7, pp. 1895–1903 , Jul. 2011.

[3] J. W. Han, J. H. Kim, S. H. Cheon, J. O. Kim, and S. J. Ko, "A novel image interpolation method using the bilateral filter," *IEEE Trans. Consum. Electron.*, vol. 56, no. 1, pp. 175–181, Feb. 2010.

[4] X. Zhang and X. Wu, "Image interpolation by adaptive 2-D autoregressive modeling and soft-decision estimation," *IEEE Trans. Image Process.*, vol. 17, no. 6, pp. 887–896, Jun. 2008.

[5] F. Cardells-Tormo and J. Arnabat-Benedicto, "Flexible hardware-friendly digital architecture for 2-D separable convolution-based scaling," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 7, pp. 522–526, Jul. 2006.

[6] S. Ridella, S. Rovetta, and R. Zunino, "IAVQ-interval-arithmetic vector quantization for image compression," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 12, pp. 1378–1390, Dec. 2000.

[7] S. Saponara, L. Fanucci, S. Marsi, G. Ramponi, D. Kammler, and E. M. Witte, "Application-specific instruction-set processor for Retinexlink image and video processing," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 7, pp. 596–600, Jul. 2007.

[8] P. Y. Chen, C. C. Huang, Y. H. Shiau, and Y. T. Chen, "A VLSI implementation of barrel distortion correction for wide-angle camera images," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 1, pp. 51 –55, Jan. 2009.

[9] M. Fons, F. Fons, and E. Canto, "Fingerprint image processing acceleration through run-time reconfigurable hardware," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 12, pp. 991–995, Dec. 2010.

[10] C. H. Kim, S. M. Seong, J. A. Lee, and L. S. Kim, "Winscale : An imagescaling algorithm using an area pixel model," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 13, no. 6, pp. 549–553, Jun. 2003.

[11] C. C. Lin, Z. C. Wu, W. K. Tsai, M. H. Sheu, and H. K. Chiang, "The VLSI design of winscale for digital image scaling," in *Proc. IEEE Int. Conf. Intell. Inf. Hiding Multimedia Signal Process.*, Nov. 2007 , pp. 511–514.

[12] P. Y. Chen, C. Y. Lien, and C. P. Lu, "VLSI implementation of an edgeoriented image scaling processor," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 9, pp. 1275–1284, Sep. 2009.

[13] C. C. Lin, M. H. Sheu, H. K. Chiang, W. K. Tsai, and Z. C. Wu, "Real-time FPGA architecture of extended linear convolution for digital image scaling," in *Proc. IEEE Int. Conf. Field-Program. Technol.*, 2008 , pp. 381–384.

[14]   C. C. Lin, M. H. Sheu, H. K. Chiang, C. Liaw, and Z. C. Wu, "The efficient VLSI design of BI-CUBIC convolution interpolation for digital image processing," in *Proc. IEEE Int Conf. Circuits Syst.*, May 2008 , pp. 480–483.

[15]   S. L. Chen, H. Y. Huang, and C. H. Luo, "A low-cost high-quality adaptive scalar for real-time multimedia applications," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 21, no. 11, pp. 1600–1611, Nov. 2011.

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