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Research Article
Design and Performance Analysis of Configurable Logic Block of FPGA

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Keywords
Configurable Logic Block (CLB), Field Programmable Gate Array (FPGA), Buffer Logic (BL), Look Up Table (LUT).

Abstract

This paper proposes the design of a FPGA Configurable Logic Block (CLB) using Buffer Logic. Existing method CLB is designed by using flip flop. It contains more logic gates, so the device utilization is high and the speed of the circuit is reduce. In this proposed method buffer circuit is replacing instead of flip flop, so the delay of the circuit is reducing then the speed is increasing. The CLB is used to implement the logic functions. It contains 8 input LUT (Look Up Table), buffer circuit and multiplexer. The proposed CLB operation is faster than the existing one because of the device utilization is less, so that the delay is reduced .CLB is simulated at the gate level by using Xilinx ISE.

Introduction

Digital designs have been the primary focus of the speed of the system. A buffer has only a one input and a one output with behavior that is the opposite of a not gate. In a Boolean logic simulator, a buffer is mainly used to decrease the delay. In a real-world circuit, a buffer can be used to amplify a signal if its current is too weak. Buffer is used to get the output as a input. The Basic Buffer logic circuit is as shown in Figure 1.

Field-programmable gate arrays (FPGAs)[1] have established attractive point on the trade-off spectrum between the flexibility and low cost of software and the performance of hardware. In some cases, the best of both can be achieved as early researchers demonstrated a combination of a conventional. Computer with an array of FPGAs that outperformed all existing implementations of a real applications in both performance and cost.

Field Programmable Gate Array is one of the types of Complex Programmable Logic Device (CPLD). FPGAs on the other hand take less than a minute to configure FPGAs continue to be effective, especially for data-intensive applications. FPGAs have two main types of programmability: Programmable logic blocksand Programmable interconnect. Although these two features are frequently combined, either feature by itself is sufficient. Lookup Tables (LUTs) have been the backbone of FPGA logic blocks since the invention of FPGAs in the 1980s. A K-LUT is an one-output memory with K address lines that can implement any Boolean function that uses up to K variables. The earliest FPGAs used 4-LUTs, established as the best LUT size to increase area efficiency. State of the art FPGAs are pointed towards speed. Interconnect in FPGAs is slow as compared with custom ASICs, due to the presence of programmable routing switches and the overheads enforced by programmability.

The objective of this work is to design and analysis the performance of CLB[2] using Buffer logic. In particular, this paper presents the design, analysis of the performance and simulation of a Buffer based configurable logic block (CLB). The design has not been fabricated. However, simulation using Xilinx ISE predicts correct operation.

Theory

A configurable logic block (CLB) is one of a basic block of an FPGA. The basic Configurable Logic Block has Lookup Table(LUT), Flip-Flop and Multiplexer. It is the most important Logic Element in FPGA.This provides the basic logic and storage functionality for a target application design. In order to furnish the basic logic and storage capability, the basic element can be either a transistor or an entire processor. Nevertheless, these are the two extremes where at one end the basic element is more fine-grained (in case of transistors) and

requires high amount of programmable interconnect which finally results in an FPGA that endures from area-inefficiency, low performance and high power consumption. On the next end (in case of processor), the basic logic block is more coarse-grained and cannot be used to implement small logic functions as it will lead to loss of resources.

Among these two extremes, there exists a spectrum of canonic logic blocks. Some of them include logic blocks that are made of NAND gates; an interconnection of MUX, lookup table (LUT) and Programmable Array Logic style wide input gates. Some vendors like Xilinx [3] and Altera[3] use LUT-based CLBs[3] to furnish basic logic and storage functionality. LUT-based CLBs provide a good trade-off between too fine-grained and too coarse-grained logic blocks. The basic LUT based CLB Architecture is as shown in the Figure 2.

Existing method

There have been a number of asynchronous FPGAs developed over the few decades. The important basic block in FPGA is Configurable Logic Block (CLB). The basic CLB consists of Look Up Table (LUT)[2], Flip Flop and Multiplexer, which is shown in the figure 2. The configurable Logic block is used to implement the Logic Function. I=AB+CD+EF+GH logic function have been implemented in this CLB. The same logic function would be implemented in the proposed CLB also.

In that existing CLB architecture contain D-Flip Flop. It has more logic gates and device utilization is high. So that the delay is high and speed of the circuit is less.

Design of CLB

The proposed CLB design supports 8 logical input variables (A, B, C, D, E. F, G, H)[2] and supports one output (i). I=AB+CD+EF+GH logic function would be implemented in this CLB Fig.4 shows CLB Architecture block diagram. The CLB consists of: Static LUT, Buffer, and Programmable Mux.

In that existing CLB architecture contain D-Flip Flop. It has more logic gates and more device utilization. So that the delay is high and the Speed would be reduced. That's why replacing Buffer instead of Flip-Flop.

However an input and an output of D-Flip Flop and Buffer is same. Buffer has only two gates, so the device utilization is less compared to Flip-Flop. Thus the device gets less delay and high Speed. A more efficient configurable logic block for a Field Programmable Gate Array was presented in this paper.

A.LUT

It stands for Lookup Table, Which is an array that reduces the computation time. Lookup Tables may be pre-calculated and stores the values in some places often it is taken and performs the operation. So it is used to save more time.

Buffer

A buffer has only a one input and a one output with behavior that is the opposite of an NOT Gate. It simply passes its input, unchanged, to its output. In a Boolean logic simulator, a buffer is mainly used to decrease the delay. In a real-world circuit, a buffer can be used to amplify a signal if its current is too weak. Buffer gate and the truth table for that is as shown in the fig.6

Result

The Proposed CLB operation is faster than the existing one because it has less number of gates and device utilization is less, so that the delay is reduced and the speed of the circuit would be increased. The Proposed and Existing Configurable Logic Blocks Performance analysis and the device utilization are tabulated in Table[1]. The CLBs has been simulated and measured their delays and device utilization by using Xilinx ISE 12.1 and ModelSim.

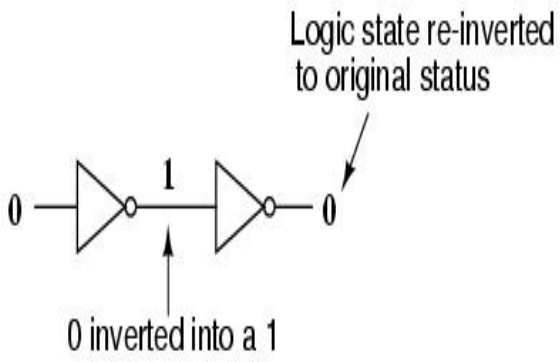


Figure.1: Buffer logic

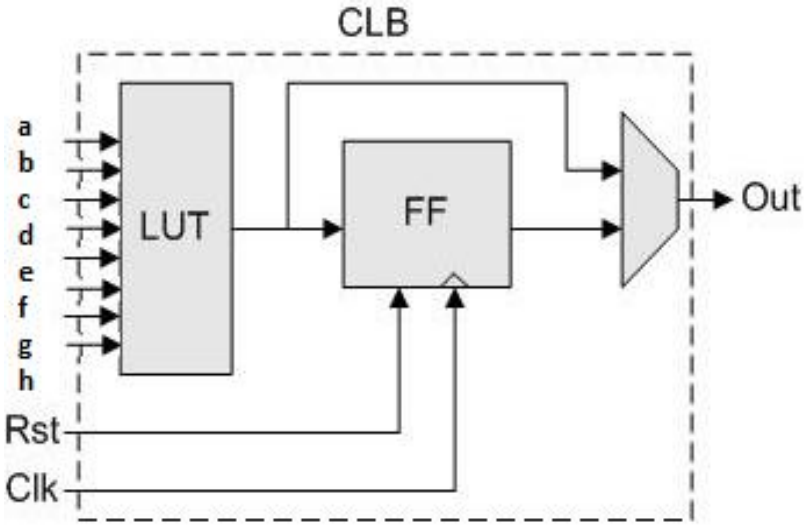


Fig. 2: Basic CLB Architecture

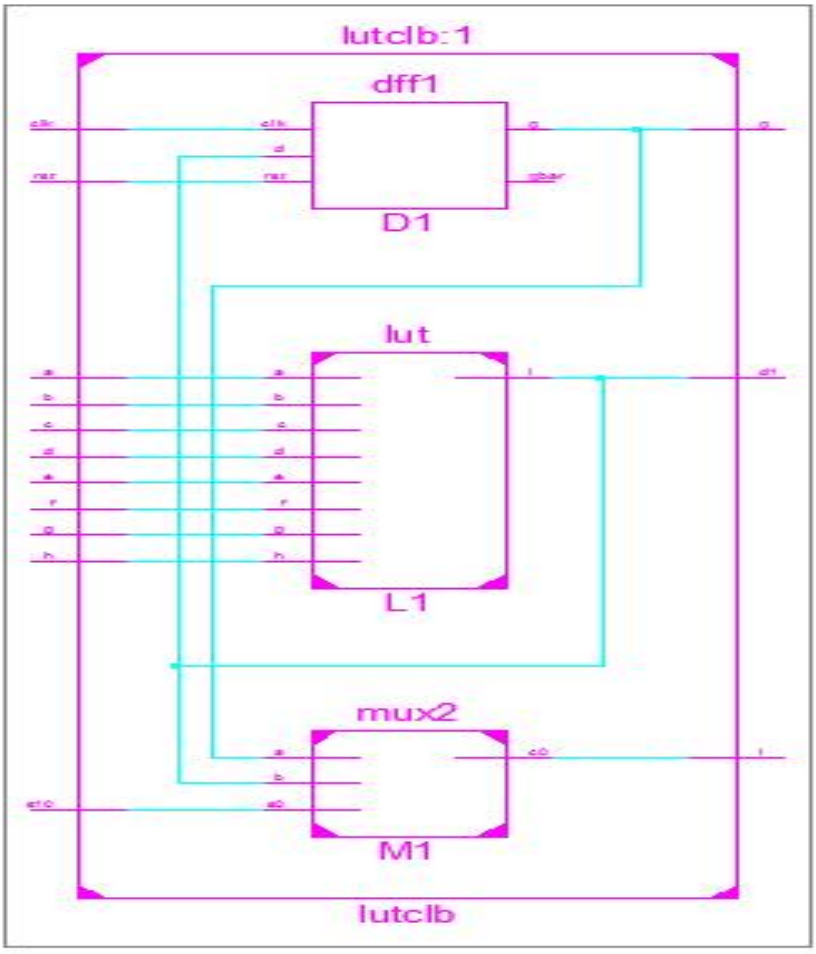


Fig.3: Existing CLB architecture RTL Schematic

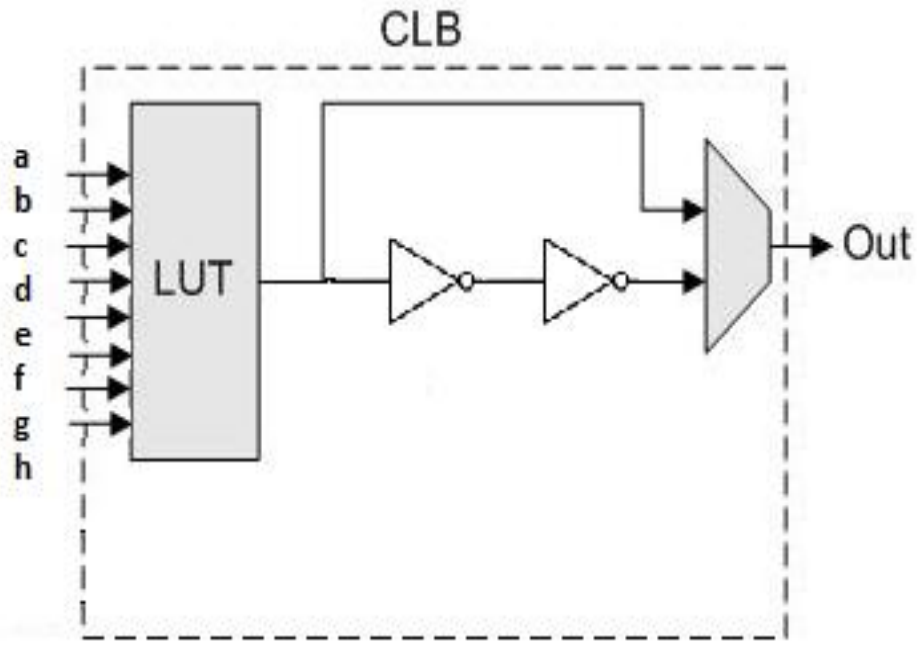


Fig 4: Proposed CLB Architecture

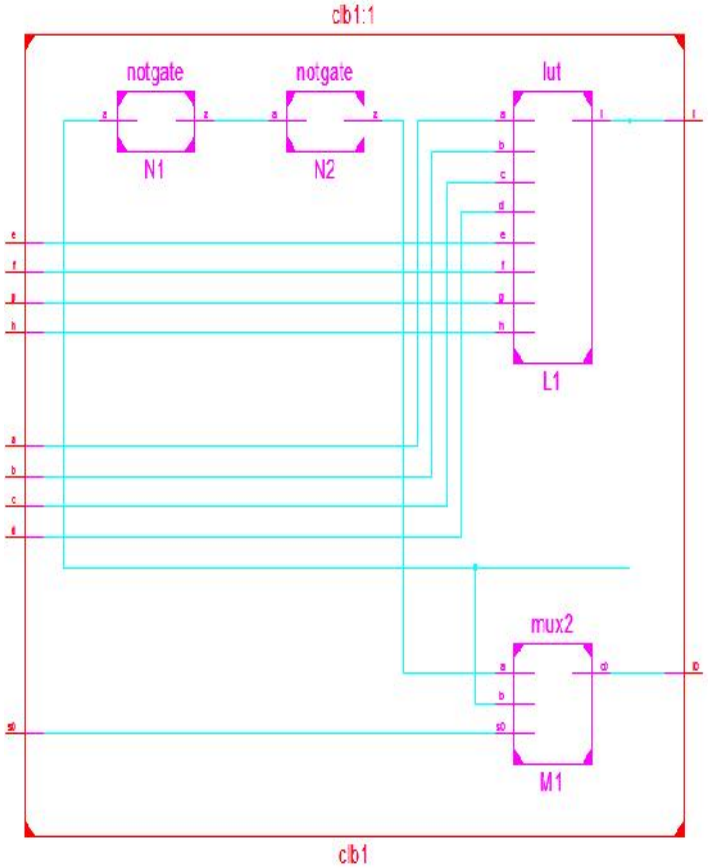
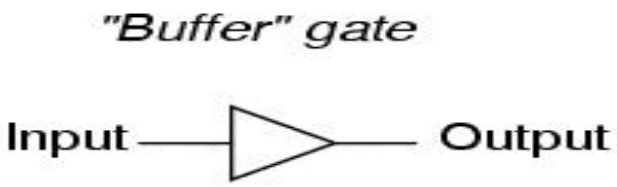


Fig.5: Proposed CLB architecture RTL Schematic



Input	Output
0	0
1	1

Fig.6: Buffer gate and truth table

Table 1: CLB Performance Analysis:

Factors	Existing	proposed
Device Utilization	1.Number of Slices:2 2.Number of IOs: 14 3. Number of bonded IOBs:11	1.Number of Slices:2 2.Number of IOs:13 3.Number of bonded IOBs:10
Combinational Path Delay	7.619[ns]	7.203[ns]
Net Delay	IBUF:1.218 LUT4:0.704 MUX:0.321 OBU:3.272	IBUF: 0.849 LUT:0.648 MUX:0.276 OBUF:3.127
XST Compilation Time	6.00 secs	5.00 secs

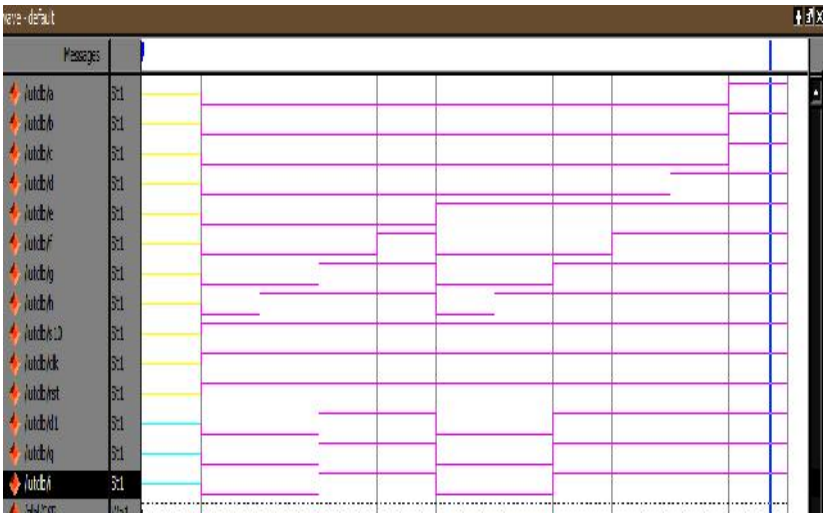


Fig.7: Output waveform of FF Based CLB

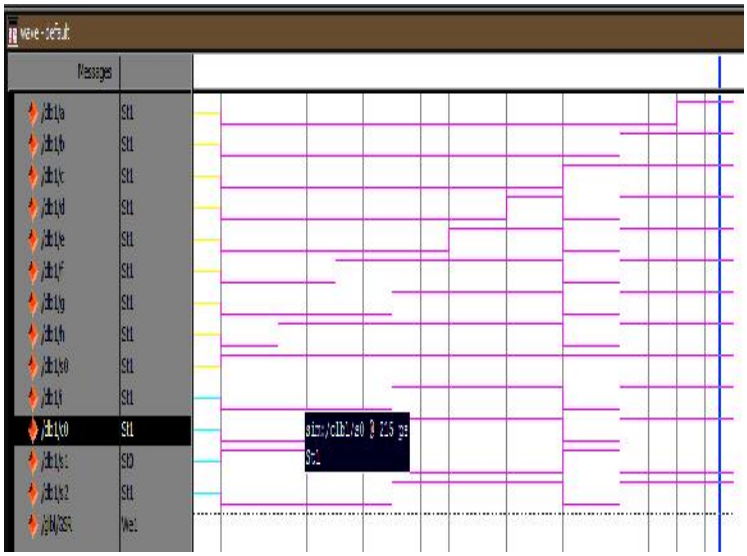


Fig.8: Output waveform of Buffer Based CLB.

Conclusion and future work

The CLB was configured for the different outputs and was successfully simulated and verified to be functionally correct. Also the results can be verified for further complex configurations. Additional topics that need further investigation, but are beyond the scope of this paper, include the overall FPGA architecture, switching matrix, and the FPGA interconnect strategy. Possible choices for overall architecture include island-style or hierarchical. Alternative numbers of LUTs and connection of LUTs within a CLB need to be studied. The overall FPGA interconnect grouping needs to be researched.

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